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For: **CIRCUITS ASSOCIATED WITH FUSIBLE ELEMENTS FOR ESTABLISHING AND DETECTING OF THE STATES OF THOSE ELEMENTS**

APPLICATION FOR UNITED STATES

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CIRCUITS ASSOCIATED WITH FUSIBLE ELEMENTS FOR ESTABLISHING AND DETECTING OF THE STATES OF THOSE ELEMENTS

FIELD OF THE INVENTION

[0001] The present invention relates to circuits for use with fusible elements and more particularly to such circuits for use with fusible elements permanently storing information on semiconductor chips.

RELATED APPLICATIONS

[0002] This application is related to United States Patent Application Ser. No. 10/XXX,XXX, Attorney Docket No. POU920020139US1, entitled CIRCUITS ASSOCIATED WITH FUSIBLE ELEMENTS FOR ESTABLISHING AND DETECTING OF THE STATES OF THOSE ELEMENTS, by Seth Erlebacher et al. These co-pending applications and the present application are owned by one and the same assignee, International Business Machines Corporation of Armonk, New York. The descriptions set forth in these co-pending applications are hereby incorporated into the present application by this reference.

[0003] Trademarks: IBM ® is a registered trademark of International Business Machines Corporation, Armonk, New York, U.S.A. S/390, Z900 and z990 and other product names may be registered trademarks or product names of International Business Machines Corporation or other companies.

BACKGROUND OF THE INVENTION

[0004] In the fabrication of electrical circuits on semiconductor chips, processing variations often prevent the fabrication of components to the precision needed in large arrays. Those arrays use fusible elements in circuits to identify semiconductor chip types and in connection with redundant circuit elements to repair the arrays after fabrication by

excluding bad elements and including substitute circuit elements. In chip identification circuits, the chip type is identified by the state of a plurality of the fusible elements where certain of the elements are blown to leave an open circuit while others are left conductive so that together fusible elements form a binary number that distinctively identifies the chip type. The binary number can then be read by applying voltage to the circuits containing each fusible element. Because of the above mentioned processing variations, circuit component differences make it very difficult for a detection circuit to detect whether a fuse circuit is open or conductive. Thus a chip whose part number is 010 could be misread as part number 011 due to the inability of the detection circuit to distinguish between an open and conductive fuse circuit for the least significant figure. Parity checking can be used to determine if an error has occurred in the case of the simple three bit binary number discussed above. However, in the reading out of a multicharacter chip identification number where each character is an 8 bit byte, multiple errors could require a sophisticated multiple error correcting system to locate and correct errors which in turn requires the use of valuable chip real estate. Further, the personalization of the fusible elements involves the use of high currents and voltages which could damage the detection circuits used in the detecting the state of the fusible elements and other circuits on the chip.

BRIEF SUMMARY OF AN EXEMPLARY EMBODIMENT

[0005] Disclosed herein in an exemplary embodiment is an identification circuit for establishing and sensing the state of a fusible element used in on chip identification of the chip's type comprising: a circuit establishing control signals for turning the identification circuit on and off for sensing with an initiating signal which signal remains off during the personalization of the fusible element; dual paths energized by the control signals generated by the level setting circuit to energize one path through the fusible element to provide a state level and the other path through a reference path which

provides a reference voltage level which is distinguishable from both the blown and unblown states of the fusible element; a differential sensing circuit for comparing the reference voltage level to the state level to provide a signal indicating the state of the fusible element; and protection circuitry changing voltage levels on the dual paths and the differential sensing circuit to protect the circuit during an operation in which the state of the fusible element is set.

[0006] A feature of an exemplary embodiment is that the state detection circuit for each fusible element includes a differential sensing circuit that compares voltage at a detection point in a path containing the fusible element with that at a reference point in a path establishing a non-zero reference voltage. The two paths are similarly configured except one contains the fusible element while the other contains a device establishing the reference voltage. The two paths for any given sensing circuit are located in close proximity to each other so that even though element parameters in the paths of different sensing circuits may vary significantly, those values track each other in the given sensing circuit. As a result, the normal non-zero value of the voltage at the reference point maintains a relationship to that at the detection point that enables the differential sensing circuit to detect between a blown and an unblown element irrespective of variation in circuit element parameters. In order to prevent detection circuits and other circuits on the chip being damaged, during blowing of the fusible elements, devices of the sensing circuits are chosen to isolate the detection circuits from the other circuits on the semiconductor chip and the excitation levels applied to the detection circuits are raised to maintain differential voltages in the detection circuits at sufficiently low levels to prevent damage.

[0007] Yet another feature of an exemplary embodiment is providing new detection and control circuits for use with electrically blowable fusible elements on semiconductor chips. More particularly, providing such circuits which accurately detect

the fusible elements state and prevent damage to the detection and other chip circuits during the blowing of such elements. Finally, yet another feature of an exemplary embodiment is providing a fusible circuits for use in chip identification and redundancy circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] These and other objects and advantages of the present invention may be best understood by reading the accompanying detailed description of the exemplary embodiments while referring to the accompanying figures wherein like elements are numbered alike in the several figures in which:

[0009] Figure 1 is a schematic representation of a semiconductor chip containing fusible elements identifying the chip type;

[0010] Figure 2A is an electrical schematic for the level and current generating circuits for activating the sense circuits;

[0011] Figure 2B is an electrical schematic of circuits for establishing and comparing the state of the fusible element;

[0012] Figure 2C is an electrical schematic of circuits for reading and retaining the state;

[0013] Figure 3A is a schematic diagram showing a plot of typical applied and output voltages of the circuit of Figures 2A to 2C during the detection of the state of a fusible element; and

[0014] Figure 3B is a schematic diagram showing a plot of typical applied and output voltages during the personalization of the fusible elements.

[0014] The detailed description explains the preferred embodiments of our invention, together with advantages and features, by way of example with reference to the drawings.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0015] Referring now to Figure 1, a semiconductor chip 100 is shown as containing a plurality of areas 102 each of which contains a fusible element 104 with the circuits illustrated Figures 2A to 2C associated with that particular fusible element. As can be seen, while a fusible element and its associated circuits can be located in any area of the chip, the fusible element, and its associated circuitry, are located in close proximity to each other. The size of the areas 102 are shown out of proportion to the chips size. The circuits actually use only a small portion 106 of the chip real estate.

[0016] The fusible elements 221 are arranged in sets of eight digits, one of which is a parity check digit, to identify one character in the chip's identification number. The chip will contain many such groups of 8 in order to provide an appropriate alphanumeric sequence to identify the chip type. An output representing the state of each fusible element can be determined by the state of latches 108 associated with that element when the detection circuits are interrogated. The chip identification samples can then be read out by shifting the bits representing the states of all the digits out on shift register 110 formed of the latches. In an exemplary embodiment the fusible element 221may be formed of a polysilicon semiconductor or equivalent material. It will be appreciated that other materials are possible, for example selected metals and the like may also be employed to form the fusible element 221.

[0017] Referring now to Figure 2A, the INIT input to the gates of N-FET devices 200 and 202 controls the activation of the sensing circuit of Figure 2B. The INIT input 200 is down at all times except during the occurrence of a sensing sequence. This means

that the INIT input is not only down when the sense circuit is not in use, but also when the fusible element is being personalized. During the time that the INIT signal is down, the TIE and MIRROR reference voltages are at substantially V1 voltage. When the INIT voltage is on or positive it provides a positive voltage at the gates of both the 200 and 202 devices. As a result, current flows from V1 to ground through FET device 200 and resistors 204, 206, 208, and 210 to establish the positive TIE reference voltage, and current flows through devices 202 and FET devices 212 and 214 to establish a positive MIRROR voltage. The TIE reference voltage is used to gate on FET 214 and the gate of FET 212 is set at the MIRROR voltage level so that MIRROR voltage tracks the TIE voltage. All the elements of the reference setting circuits are physically located in close proximity to each other so that the characteristics of devices 200 to 214 track each other to maintain the difference between the TIE and MIRROR voltages within desired limits.

[0018] Referring now to Figure 2B, the MIRROR reference voltage is provided to the gates of P-FET devices 215 and 216, while the TIE reference voltage is provided to the gates of P-FET devices 218 and 220. Devices 215 and 218 are connected in a path containing the fusible element 221 and N-FET devices 222 and 223. While devices 216 and 220 are connected in a path with N-FET devices 224 and 225 and resistive element 226. Because of proximity of the devices on the chip, characteristics of like devices in both paths are substantially the same. The paths are connected in parallel between the voltage sources V_1 and F SOURCE. V_1 is up whenever the chip is operating while F SOURCE is at ground potential at all times the chip is operating except when the state of the fusible element 221 is being set. With the TIE and MIRROR reference voltages up, devices 215, 216, 218, and 220 are off so that the same voltage at points 227 and 228 is indeterminate because both the state and reference paths are open circuits. With devices 215, 218, 222 and 223 and 216, 220, 224 and 225 conductive, current through devices 215, 218, 222 and 223 provide a voltage at output point 227 across the fusible element

221 and semiconductor device 223 and current flowing through device 216, 220, 224 and 225 provides a fuse reference voltage to terminal 228 across device 225 and resistor 226. If the fuse is blown, a high voltage will be provided at terminal 227. If the fuse is unblown, a lower voltage will be presented at terminal 227. The reference voltage at point 228 will remain the same whether the fuse path is blown or unblown. Thus a detectable difference between the two points 227 and 228 is present between the blown and unblown state. In an exemplary embodiment, to generate a detectable voltage between points 227 and 228 reference resistive element 226 is configured to exhibit a resistance between the highest resistance value of an "un-blown" fusible element 221 and the lowest resistance value of a "blown" fusible element 221. In an exemplary embodiment, the resistive element 226 is selected to exhibit a resistance of approximately twice that of an unblown fusible element 221. Like the circuits in Figure 2A, the circuit elements of Figure 2B are arranged in close proximity to one another so that their characteristics track one another to maintain the difference of the detectable levels at terminals 227 and 228 within a desired range.

[0019] The resistive element 226 may be formed in a variety of ways, one example is via a conventional semiconductor manufacturing processes, including but not limited to buried resistor (BR) technology, diffusion resistors, polysilicon, metal, silicide, and the like, or discrete components as well as combinations including at least one of the foregoing. An improved method over these processes in accordance with an exemplary embodiment, would be to fabricate the resistive element 226 employing the same material as the fusible element 221 with characteristics closely matching that of the fusible element 221. In one embodiment, fabrication of the resistive element 226 may utilize conventional semiconductor manufacturing processes technology to make the reference resistor. In some instances this would exhibit the advantage of being a well controlled resistor with respect to tolerances, quality, and the like. In another exemplary

embodiment the resistive element 226 is configured and fabricated using the same material as the fusible element 221. When considering the desired the resistive element 226 is selected to exhibit a resistance of approximately twice that of an unblown fusible element 221. This approach results in a resistive element 226 exhibiting the same width as the fusible element 221 with a length, twice as long. Yet another option configures the resistive element 226 as two copies of the fusible element 221 connected in series, and thereby simplifying component fabrication.

[0020] Advantageously, each of these approaches yield improved circuit tracking over a standard resistance. The differential detection of the exemplary embodiments disclosed herein reduce the voltage variation required for robust sensing of a blown or unblown fusible element 221. In earlier configurations, either a larger current would need to be applied to the fusible element 221 or a longer sensing duration would be employed. Advantageously the exemplary embodiments allow for a reduction in the size of certain transistors decreasing the area occupied by the fuse circuits on the chip and/or reduced fuse blow time. These improvements enhance test productivity. Once again, in an exemplary embodiment, reference resistive element 226 is configured to exhibit a resistance between the highest resistance value of an "unblown" fusible element 221 and the lowest resistance value of a "blown" fusible element 221. By making the reference resistive element 226 or of the same material as the fuse and at least as large, it is guaranteed that the resistance thereof will be larger than that of an un-blown fusible element 221. Therefore, by careful coordination of the fabrication processes for the fusible element 221 and the resistive element 226, reference resistive element 226 may be configured to be twice as large as fuse will assure that the resistance is less than that of a blown fuse. The 2x factor also allows for tracking errors.

[0021] The first embodiment is somewhat smaller in layout than the second described above, but does not track the fuse as well as it only has the same contact

structure as the fuse, where 2 sets of contacts would be ideal. The second embodiment described above is larger in layout than the first embodiment, but has the advantage of comprising two parts/pieces, which facilitates flexibility in layout. Advantageously, the second embodiment also doubles the number of contacts.

[0022] Continuing now with FIG. 2B, with N-FET devices 230 and 232 biased conductive by a positive ENABLE BAR input and N-FET devices 234 and 236 biased non-conductive by the ENABLE BUF input, the sense outputs of 227 and 228 are provided to differential amplifier input terminals 238 and 240. As shown in Figure 2C, the sense amplifier 241 contains N-FET and P-FET devices 242 to 252. This circuit takes signals 238 and 240 and sets the level at point 254 based on the relative levels 238 and 240 and sets the level at point 254 based on the relative levels 238 and 240. If the voltage at 238 across the fusible element 221 is above that reference voltage at point 257 the device 244 conducts to provide a down voltage indicating that the fuse is not blown. If the voltage at terminal 238 is lower than the reference voltage 252, then device 244 will not conduct providing an up voltage at output terminal 254.

[0023] The voltage at output terminal 254 is received by a double inverter circuit 256. Devices 258 to 264 of circuit 256 take the signal 254 and increases its level margins. The latch circuit 268 comprises AND circuit 270, NOR circuits 272 and 274 and an invert circuit 276. Latch 268 is triggered into operation by the INIT signal to store the signal representing the state of the fusible link by feeding a positive INIT input into the AND circuit 270 along with the fusible link state information at point 266. The NOR circuits 272 and 274 latch the state generated at point 266 while the invert circuit 276 inverts the latched signal so that a positive output indicates that an open fusible element results in a binary "0" output while a down output results in a binary "1" output. Again the circuit elements of the differential amplifier are in close proximity to one another so that the

elements track each other maintaining the relevant values between the fuse and unfused state.

[0024] Above described is the sensing of the state of an element which is fused or unfused during a previous fusing operation. As can be seen referring back to Figure 2B, the fusing of the element is accomplished by applying an increased voltage across the fusible element 221. For this purpose, a NOR circuit 280 is connected to the gate of NPN device 281 which is connected in series with the fusible element and device 223 between ground and the F SOURCE terminal. The F SOURCE voltage 258 is always increased from ground potential during the personalization operation. Whether the element 221 is to be fused is determined by the BLOW and ENABLE BAR inputs to the NOR circuit 280. If the BLOW signal is down at the same time as the ENABLE BAR circuit is down, the NOR circuit 260 raises the gate voltage on N-FET device 281 providing sufficient current through transistors 223 and fusible element 221 to blow out fusible element 221 leaving an open circuit across the fusible element 221. If the BLOW signal is up while the ENABLE BAR signal is down, the NOR circuit 280 provides a down level to device 281 so that devices are nonconductive and as a result, the path between the F SOURCE terminal and ground voltage is open and the fusible element remains conductive.

[0025] In addition to its use in the blowing fuse the F SOURCE voltage is applied to gates of N-FET devices 283 and 282 through resistors 284 to 287 to prevent circuit elements of the chip from being affected by the high F SOURCE voltage. At the same time the ENABLE BAR voltage is reduced to turn devices 222, 224, 230 and 232 off. Further, ENABLE BAR voltage is used to short the terminals 238 and 240 to ground through devices 234 and 236 and to turn on devices 288 and 289 to isolate the fusible element in reference circuits from other elements on the circuit chip. Figures 3A and 3B

contain the voltage patterns during the detection and personalization of the fusible elements, respectively.

[0026] It will be appreciated that the use of first and second or other similar nomenclature for denoting similar items is not intended to specify or imply any particular order unless otherwise stated.

[0027] While we have described an embodiment of the invention, those skilled in the art may or may not anticipate changes in this embodiment. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. For instance, as mentioned above, while the above described embodiment deals with storing information on semiconductor chips, the fusible element circuits can also be used in connection with the use of redundant circuits. Therefore it should be understood that the invention is not limited to this embodiment disclosed as the best mode contemplated for carrying out this invention, but covers it and other embodiments within the intent and spirit of the attached claims.